NBS TECHNICAL NOTE **1105**

U.S. DEPARTMENT OF COMMERCE / National Bureau of Standards

A 20 Bit + Sign, Relay Switched D/A Converter

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Contents

A 20 BIT + SIGN, RELAY SWITCHED D/A CONVERTER

T. Michael Souders
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A multirange, 20-bit + sign, voltage output D/A converter is described. The converter exhibits less than 1 ppm (of full scale range) linearity error, and temperature coefficients of gain, offset and linearity of less than 0.5 ppm/°C. The design is based on the R-2R ladder network in the current steering mode, using miniature latching relays with mercury wetted contacts for switching. Ten buffered, temperature-controlled unsaturated standard cells comprise the voltage reference.

Techniques with design details are presented for minimizing errors due to relay thermal emf's, for implementing a self-calibration of linearity errors, and for obtaining optional coding formats. Calibration techniques are discussed and representative calibration data are presented.

Key Words: Digital-to-analog converter; high resolution; multirange; R-2R ladder; relay switching; self-calibration; twenty bits + sign; voltage output.

INTRODUCTION

In 1975 a new program was initiated at the National Bureau of Standards to provide measurement support for the burgeoning electronic instrumentation industry. An initial requirement of the program was for an accurate, digitally programmable voltage source to serve as a reference standard. High resolution, linearity and stability, as well as ease and flexibility of operation were the primary performance requirements. A D/A converter having the following specifications was developed to meet these criteria.

- Code Format - Binary Sign-Magnitude, with BCD option requiring external code converter. TTL compatible inputs.
- Voltage Ranges - ±10 V, ±5 V, ±2.5 V and ±10 V BCD for use with code converter.
- Resolution - 20 bits + sign, i.e., 10 μV, 5 μV and 2.5 μV respectively on the 10 V, 5 V and 2.5 V ranges, bipolar or unipolar.
- Conversion Rate - 100/s, max.
- Linearity - Less than 1 ppm of Full Scale Range (±10 V) after self-calibration.

• Temperature Coefficients (gain, offset, linearity) - less than 0.5 ppm/°C each, near room temperature.

A self-calibration feature has been included which permits the linearity of the eight most significant bits to be measured and adjusted if necessary.

DESIGN CONSIDERATIONS

The basic R-2R ladder network, used in the current switching mode (Fig. 1), was selected for this design [1]. It has the advantages of having only two binarily related resistor values, low voltage current switching, constant power dissipation in the resistors regardless of switch positions, as well as easy implementation of a self-calibration technique.

Polarity and Range Selection

A schematic diagram illustrating a more complete implementation is given in Fig. 2. Polarity and range switching precede the ladder, before the reference voltage is attenuated. These functions are accomplished with amplifier circuits A1 and A2, and their respective switches S_P and S_R. The magnitudes of the two reference polarities are matched by adjusting the offset voltage of amplifier A1 with a panel accessible trim potentiometer not shown in the figure. Gain adjustment is accomplished by injecting a variable current into the summing node of A2. As this current is always of the same polarity as the main input current through R_{IN}, the exact value of R_{IN} which is nominally $(1.019)\cdot(2R)$, is chosen appropriately to produce an initial negative gain error of approximately 100 ppm. When properly offset, the gain may be adjusted by 100 ppm in both directions by varying Pg.

Ladder and Trimming Circuits

The ladder resistance R was chosen to be $10^4\Omega$, optimizing the tradeoff between errors due to amplifier performance, leakage resistance, and switch and wiring resistance. The resistors are etched bulk metal of a proprietary design. For the most critical applications (polarity, range, eight most significant ladder bits and output) the resistors are hermetically sealed in miniature (1 cm x 1 cm x 0.3 cm) oil-filled cans. These have been matched to better than 10 ppm and exhibit temperature coefficients of ±1 ppm/°C and tracking temperature coefficients of ±0.5 ppm/°C. The quality and tolerances of resistors used in less critical positions were chosen accordingly.

Operational amplifiers A1 - A3 require performance consistent with 20 bit (1 ppm) accuracy, i.e., open-loop gain in excess of 120 dB, very low offset voltage drift with time and temperature, low offset and bias currents, low noise, and for A3, settling time (including thermal tails) of less than 1 ms (see Appendix). Amplifier A4 used in the self calibration circuit described later, requires in addition, a high common

mode rejection ratio and very high input impedance (>$10^{11}\Omega$). Offset adjustments are available from the front panel for each of these amplifiers.

Bit trimming circuits are provided for adjusting the eight most significant bits using a non-interacting current injection technique. The trimming currents are driven through high impedance into the low voltage nodes shown in Fig. 2. The currents are derived from variable voltages slaved to the ladder reference voltage. With the component values shown in the figure, the total adjustment range is ±100 ppm for each bit. Twenty-turn trimming potentiometers give resolution on the order of 0.1 ppm.

Switches

For the current steering function, switches having very low and repeatable contact resistance, and relatively low thermal emf's are required. The performance sought for the most critical switches is approximately 1 mΩ contact repeatability and 1 μV/°C net thermal emf. Unfortunately, switches offering such low contact resistance generally have mercury wetted contacts and hence higher thermal emf. Miniature latching relays with mercury wetted contacts, mounted in 14 pin dual inline packages were chosen for this task. The switch design minimizes the thermal emf problem by having the junctions in close proximity, and when operated statically (without power to the coils) under normal ambient laboratory conditions exhibit thermal emf's of only 1 - 2 μV. For these same relays, however, large emf's (~150 μV) result from internal thermal gradients when the relay coils are continually energized. To minimize this problem, the relay coils are pulsed for approximately 2.5 ms, just long enough to insure that the relay has latched in the proper position. The circuit of Fig. 3 is used to produce this 2.5 ms drive pulse. Note that a dual one-shot IC is required for each relay, rather than a single one-shot to provide an enable pulse to all relays in parallel. This additional circuitry was included to ensure that each relay is pulsed when and only when the input logic changes state. Since in many applications only a single or a few bits are changed in each new word, this technique considerably reduces the average power supplied to each relay. In applications in which the D/A converter is ramped up or down one bit at a time, for example, only the least significant bit is exercised at the full word rate, and consecutively higher bits are exercised proportionately less often. Figure 4 shows representative plots of the maximum emf's developed across a relay as a function of switching rate and pulse duration. Equilibrium at the maximum values indicated was reached after about 5 min. operation at the designated switching rate.

Finding an exact expression for the resultant error contributions of the relay thermals in the general case (arbitrary distribution of thermals among the relays and arbitrary configurations of switch states) is a formidable problem. However, the results of extensive measurements and calculations indicate that the worst-case error voltage will not exceed $2.5e_R$, where e_R is the maximum thermal emf present in any relay.

This maximum occurs, for example, when continually changing between the codes 1110 1010 1010 1010 1011 and all zeros (0000 0000 0000 0000 0000), changing between all ones and all zeros gives half of the maximum error or $1.25e_R$, and changing only one bit at a time gives an error of $0.5e_R$ or less. These figures have been experimentally determined using a simulation circuit. The worst-case code contains an alternating pattern since this substantially reduces the total effective resistance in series with each ON switch. Reducing the conversion rate will, as Fig. 4 suggests, reduce e_R and hence the resulting errors, proportionately.

Voltage Reference

To achieve the greatest time and temperature stability for the reference voltage, ten unsaturated standard cells connected in series and mounted in a temperature controlled air bath were used (Fig. 5). The output from these ten cells is buffered with a FET input, low drift, high gain follower amplifier also mounted in the controlled air bath. As is shown in the figure, four-wire sensing at the load is provided to reduce the dependence on connecting leads.

BCD Coding

For a number of applications, BCD coding is more convenient than binary. The manual calibration of digital voltmeters, for example, proceeds much faster when the voltage source is decimally programmable, eliminating the need for binary-to-decimal conversion calculations. To accomodate such applications, a BCD voltage range has been provided which is used, together with an external hardwired BCD-to-binary code converter, to provide decimally coded output voltages. The additional BCD voltage range is necessary since binary full scale of 2^{20} (=1048576) is approximately 5% higher than the nearest convenient decimal full scale of 1000000. To obtain the 10.00000 V full scale output voltage for a decimal input code of 1000000 requires a range multiplication factor of $2^{20}/10^6 = 1.048576$, as indicated in Fig. 2.

Self-Calibration Circuit

The R-2R ladder network chosen makes possible the use of a simple self-calibration technique for measuring and adjusting the linearity errors (Fig. 6). With the addition of a switch to select the voltages at the nodes indicated, a follower amplifier to buffer the selected voltages, and a 2/1 resistive divider, the technique can be implemented. It is designed to compare the weight of each bit with the sum of all the less significant bits, recognizing that each bit ideally is equal to the sum of the less significant bits, plus 1 LSB. To assure the accuracy of the self-calibration technique, it must first be determined that no significant superposition errors exist [2], i.e., that the errors associated with each individual bit are code-independent, and are directly additive. An independent calibration is required to determine this.

To test the eight most significant bits (1 - 8), the technique proceeds as follows:

1. The 10 V range and positive polarity are selected.

2. Bits 1 - 8 are set to "0" (off-state) and bits 9 - 20 are set to "1". Switch S_S is set to node 8.

3. The microvoltmeter (μVM) is adjusted to zero (with its offset control), if necessary.

4. Bits 1 - 7 and 9 - 20 are set to "0", and bit 8 is set to "1".

5. The μVM should read 6.67 μV (1 LSB x divider ratio). Bit 8 is adjusted for the proper reading if in error.

6. Bits 1 - 7 are set to "0", bits 8 - 20 are set to "1", and switch S_S is set to node 7.

7. The μVM is again readjusted to zero.

8. Bits 1 - 6 and 8 - 20 are set to "0" and bit 7 is set to "1".

9. Bit 7 is adjusted for 6.67 μV on the μVM.

Proceed in like fashion measuring and adjusting bits 6 through 1 in succession. The detector is zeroed each time a new node is selected to eliminate systematic errors due to amplifier offsets, finite common-mode rejection, and errors in the resistive divider ratio.

Note that small adjustment errors made in the first few steps of this process propagate in geometric proportion as the adjustment procedure continues, so that the error in adjusting bit 8 is multiplied by 2^7 (128) when the most significant bit is adjusted. This multiplied error is primarily a gain error (rather than linearity error) and can be readjusted to zero by performing a gain adjustment after the self-calibration is completed.

For applications in which the D/A converter is used in automated test systems, this self-calibration technique can be automated as well by replacing the manual switch S_S with an electronically programmable one, and using a digital μVM or its equivalent to measure the self-calibration voltages. The technique could be used either to flag an out-of-tolerance linearity error for subsequent manual readjustment, or to compute and store error corrections to be automatically applied, either with software or hardware.

LINEARITY CALIBRATION

In a converter of this type, superposition errors can arise from several sources, and their magnitudes should be determined, particular-

ly if the self-calibration technique is to be used and relied upon for routine verification and adjustment. Typical error sources can include excessive resistance in common ground buses, and code-dependent self-heating in the output amplifier's feedback resistor. To verify the accuracy of the self-calibration technique, and to provide a means for checking the polarity bit, an independent calibration is needed.* This is conveniently accomplished by using an accurately known Kelvin-Varley Divider (KVD) as a comparison standard as illustrated in Fig. 7. The calibration procedure is as follows:

1. The DAC input code is set to "000...000", S_B, S_C and S_A are set to the UP position connecting the output of A3 to the detector. The offset voltage of output amplifier A3 is adjusted to zero (detector null).

2. The polarity bit S_P is set to "+", S_A is set to the down position, disconnecting the reference voltage, and the DAC input code is set to "111...111". The offset voltage of the range amplifier A2, as propagated to the output and measured by detector D, is adjusted to zero.

3. Switches S_B and S_C are set to the DOWN position connecting the KVD to the detector, S_A is set to the UP position reapplying the reference voltage, and the KVD is set to 0.5000000. The offset voltage of the polarity amplifier A1 is adjusted for detector null. This adjusts the polarity bit.

4. Switches S_B and S_A are set to the UP position to compare the DAC output with that of the KVD, a selected DAC input code is set, and the detector is then balanced by adjusting the KVD setting. The codes and KVD settings are recorded. All twenty major code transitions for each polarity are then measured in like fashion. Table 1 gives the first eight transitions in the first column.

5. The data is normalized by arithmetically offsetting and scaling the KVD settings to force the negative and positive endpoints to their ideal values (-9.99999 and +9.99999). The normalized data can then be compared at any code setting to the ideal value of that code, thereby obtaining linearity errors for each code setting. This has been done for the eight major code transitions of each polarity in Table 1.

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* Note that if offset binary coding is used instead of sign-magnitude, the polarity bit would automatically be included in the self-calibration routine.

OPTIONAL OFFSET BINARY CODING

If even greater code format flexibility is desired, the modifications made in Fig. 8 will add an offset binary coding capability. When the code selector switch is in the sign-magnitude position, the two paralleled resistors return the configuration to that of Fig. 2. In the offset binary mode, amplifier A6 introduces the necessary offsetting voltage. The sign bit switch S_p in this mode normally remains in the "+" position, although complementary coding will result simply by reversing the sign. Since this sign bit is no longer used, the resolution with offset binary coding is half that of bipolar sign-magnitude, i.e., $\frac{1}{2^{20}}$ vs $\frac{1}{2^{21}}$. If implemented, the self-calibration circuit must still be used in the sign-magnitude mode, although the calibration should be valid in the offset binary mode as well, with the added advantage of the new sign bit (bit 1) being included in the calibration.

CONCLUSION

The completed instrument (less the standard cells reference) is shown in the photograph of Fig. 9. The digital input code is displayed in the upper left corner with LED's driven from the input latches. Screwdriver access to all critical trimming potentiometers, including gain, sign-bit, offsets, and eight most significant bits, is provided from the front panel. The self-calibration mode selection switch is seen near the center of the panel. Terminals are available for output voltage, ladder reference voltage, and the self-calibration test voltage.

The instrument, designated NBS DAC-20, has been in use for nearly three years, serving as a reference standard in both manual and automatic test systems for evaluating high resolution digital voltmeters, A/D converters and D/A converters [3]. During this time DAC-20 has exhibited linearity stability of approximately 2 ppm/yr., so that the self calibration interval should be six months to maintain 1 ppm linearity. The observed zero offset stability has been even better. No direct information is available for the gain stability since the gain is frequently adjusted in service to match that of instruments under test.

During the course of these applications, an additional advantage of using relay switching has become apparent. The inherent isolation afforded between analog and digital commons greatly reduces problems resulting from analog-to-digital ground loops, which can otherwise be severe when making automated measurements with ppm resolution.

APPENDIX

The settling time of amplifier A3 can be measured with the circuit of Fig. 10. A clean 50 Hz squarewave signal is applied to the amplifier under test, and the settling waveform is viewed at the settling node marked s, with a high resolution oscilloscope. The time required after an input voltage transition for the voltage at node s to settle to and remain within 1/2 (due to the divider ratio) the desired error band is the settling time. Note that the final "settled" voltage will depend on the amplifier's offset voltage as well as on the match between the resistors R_i and R_f making up the divider. Schottky diodes are provided to clamp the settling node to ±0.5V to protect the oscilloscope's input amplifier from excessive overload. It is important to select an input amplifier which can recover from the overload to the desired accuracy in less than the desired settling time of the amplifier under test.

The settling time should be measured for the maximum positive and negative voltage transitions that will be encountered, e.g., +10 V → -10 V and -10 V → +10 V. Rate related effects can also be checked by varying the frequency and duty cycle of the input waveform.

REFERENCES

[1] D. Scheingold, Ed., Analog-Digital Conversion Handbook, Norwood, MA: Analog Devices, 1972, p. II-38.

[2] J. Naylor, "Testing Digital/Analog and Analog/Digital Converters", IEEE Trans. Circ. and Syst., Vol. CAS-25, No. 7, July 1978.

[3] T. M. Souders and D. R. Flach, "An Automated Test Set for High Resolution A/D and D/A Converters", to be published in 1979 EEMTIC issue of IEEE Trans. Instrum. Meas.

TABLE 1

DAC-20 Input Code	KVD Setting ρ	Offset & Gain Corrected Settings [1]	Settings Normalized to ±1.0 [2]	PPM of 20 V FSR
- 1111 1111 1111 1111 1111	0.0092918	0.0000005	-0.9999990	0.0
- 0111 1111 1111 1111 1111	0.2546457	0.2500002	-0.4999997	0.4
- 1000 0000 0000 0000 0000	0.2546453	0.2499997	-0.5000006	0.3
- 0100 0000 0000 0000 0000	0.3773225	0.3749998	-0.2500004	0.2
- 0011 1111 1111 1111 1111	0.3773233	0.3750006	-0.2499988	-0.1
- 0001 1111 1111 1111 1111	0.4386619	0.4375007	-0.1249986	-0.2
- 0010 0000 0000 0000 0000	0.4386613	0.4375001	-0.1249998	-0.1
- 0001 0000 0000 0000 0000	0.4693308	0.4687503	-0.0624994	-0.3
- 0000 1111 1111 1111 1111	0.4693315	0.4687510	-0.0624980	-0.5
- 0000 0111 1111 1111 1111	0.4846662	0.4843761	-0.0312479	-0.6
- 0000 1000 0000 0000 0000	0.4846655	0.4843754	-0.0312492	-0.4
- 0000 0100 0000 0000 0000	0.4923327	0.4921877	-0.0156246	-0.2
- 0000 0011 1111 1111 1111	0.4923334	0.4921884	-0.0156232	-0.4
- 0000 0001 1111 1111 1111	0.4961671	0.4960947	-0.0078106	-0.4
- 0000 0010 0000 0000 0000	0.4961664	0.4960940	-0.0078120	-0.2
- 0000 0001 0000 0000 0000	0.4980832	0.4980471	-0.0039058	-0.2
- 0000 0000 1111 1111 1111	0.4980838	0.4980477	-0.0039046	-0.3
+ 0000 0000 1111 1111 1111	0.5019160	0.5019525	+0.0039050	+0.1
+ 0000 0001 0000 0000 0000	0.5019165	0.5019530	+0.0039060	+0.1
+ 0000 0010 0000 0000 0000	0.5038333	0.5039061	+0.0078122	+0.2
+ 0000 0001 1111 1111 1111	0.5038327	0.5039055	+0.0078110	+0.2
+ 0000 0011 1111 1111 1111	0.5076664	0.5078118	+0.0156236	+0.2
+ 0000 0100 0000 0000 0000	0.5076670	0.5078124	+0.0156248	+0.1
+ 0000 1000 0000 0000 0000	0.5153341	0.5156247	+0.0312494	+0.3

[1] Offset by -0.0092913 to bring -Full Scale to 0.0000005.

Scaled by $\frac{0.9999995}{0.997078 - 0.0092913}$

[2] Normalized to ±1.0 by multiplying x 2 and subtracting (offsetting by) 1.0.

TABLE 1 (continued)

DAC-20 Input Code	KVD Setting ρ	Offset & Gain Corrected Settings [1]	Settings Normalized to ±1.0 [2]	PPM of 20 V FSR
+ 0000 0111 1111 1111 1111	0.5153335	0.5156240	+0.0312480	+0.5
+ 0000 1111 1111 1111 1111	0.5306683	0.5312492	+0.0624984	+0.3
+ 0001 0000 0000 0000 0000	0.5306689	0.5312498	+0.0624996	+0.2
+ 0010 0000 0000 0000 0000	0.5613385	0.5625001	+0.1250002	-0.1
+ 0001 1111 1111 1111 1111	0.5613378	0.5624994	+0.1249988	+0.1
+ 0011 1111 1111 1111 1111	0.6226765	0.6249996	+0.2499992	-0.1
+ 0100 0000 0000 0000 0000	0.6226771	0.6250002	+0.2500004	-0.2
+ 1000 0000 0000 0000 0000	0.7453546	0.7500006	+0.5000012	-0.6
+ 0111 1111 1111 1111 1111	0.7453540	0.7500000	+0.5000000	-0.5
+ 1111 1111 1111 1111 1111	0.9907078	0.9999995	+0.9999990	0.0

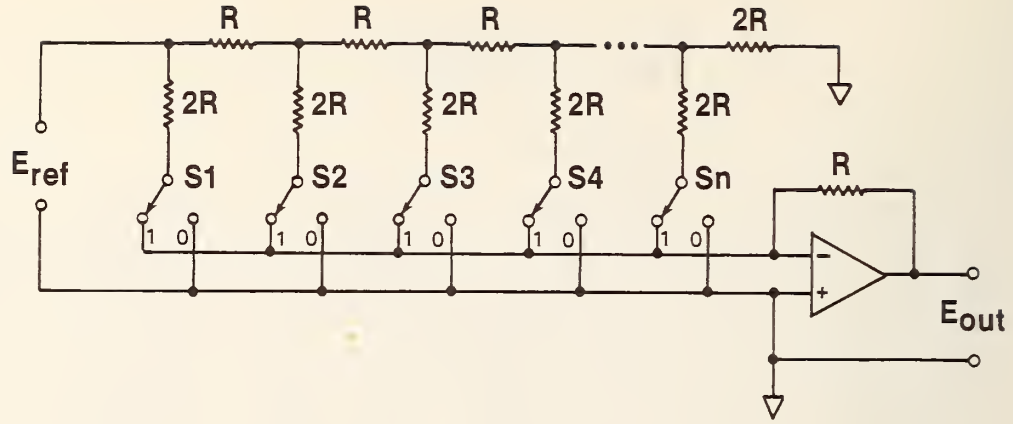

Fig. 1 R-2R Ladder Network

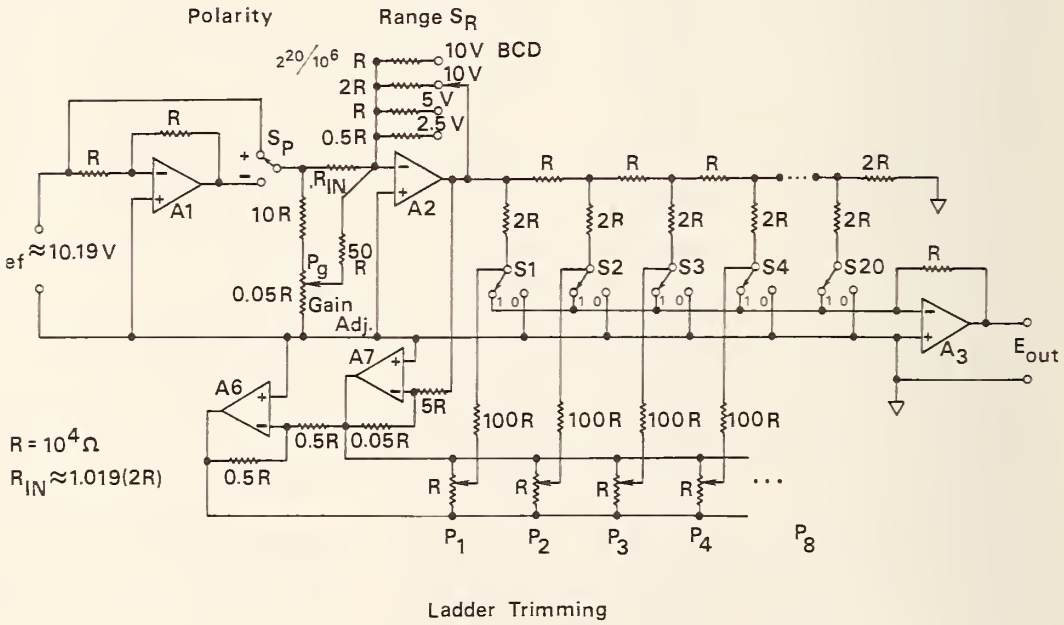

Fig. 2 20-Bit D/A Converter Circuit

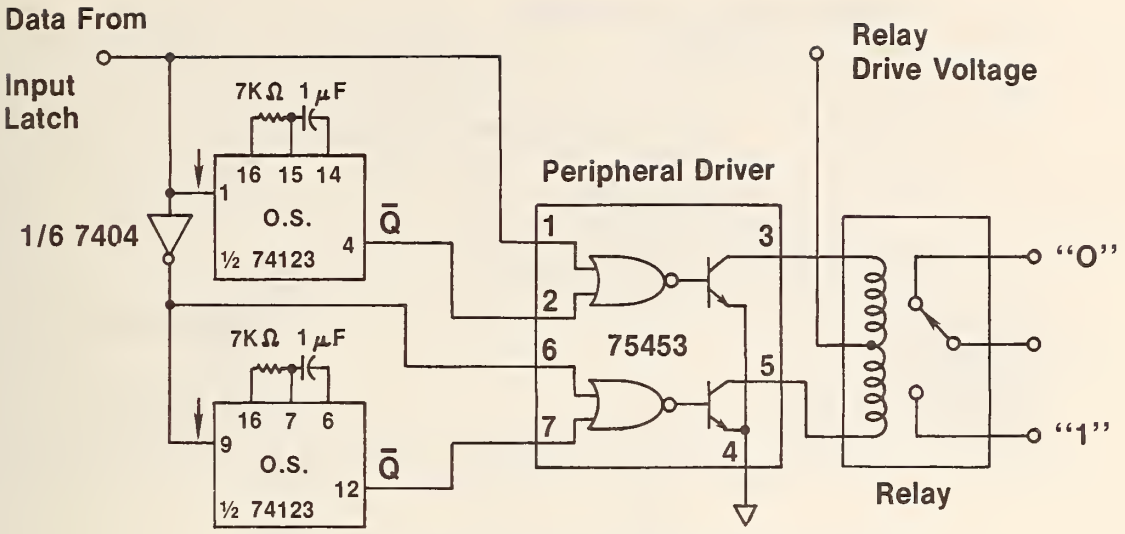

Fig. 3 Relay Logic and Drive Circuit

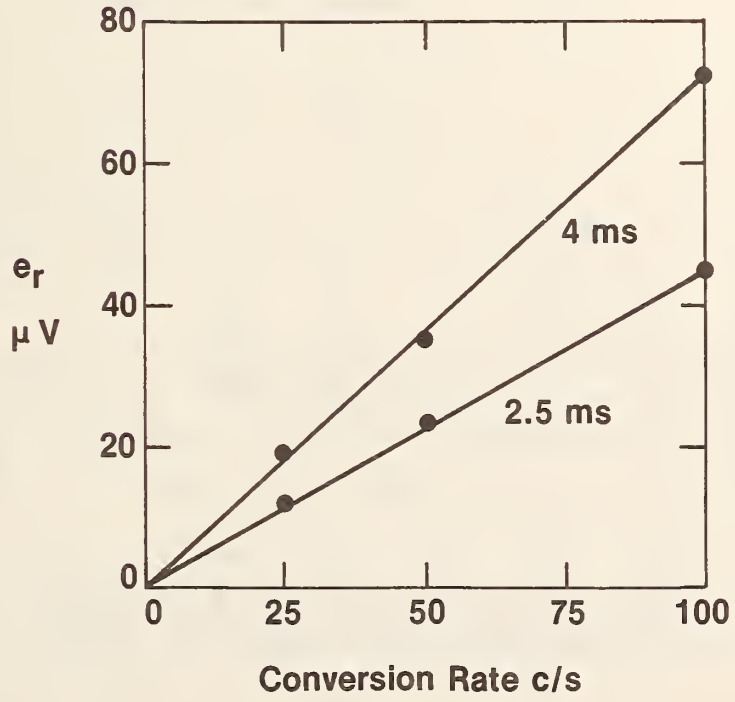

Fig. 4 Relay Thermal emf's as a Function of Switching Rate and Pulse Duration

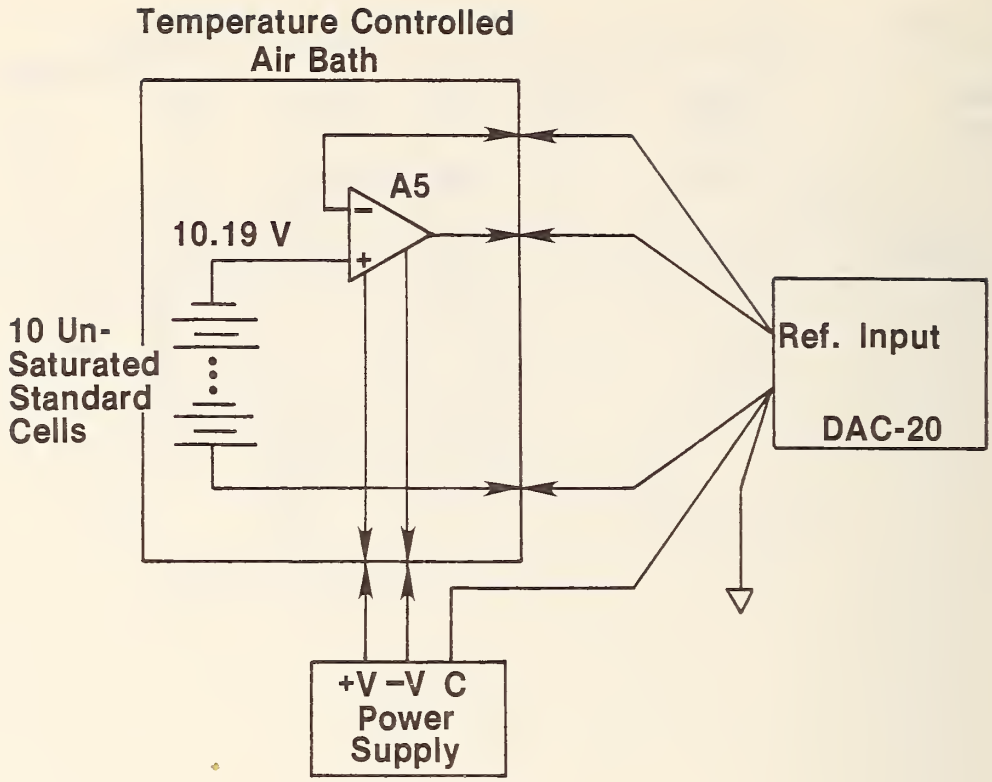

Fig. 5 Reference Voltage Supply

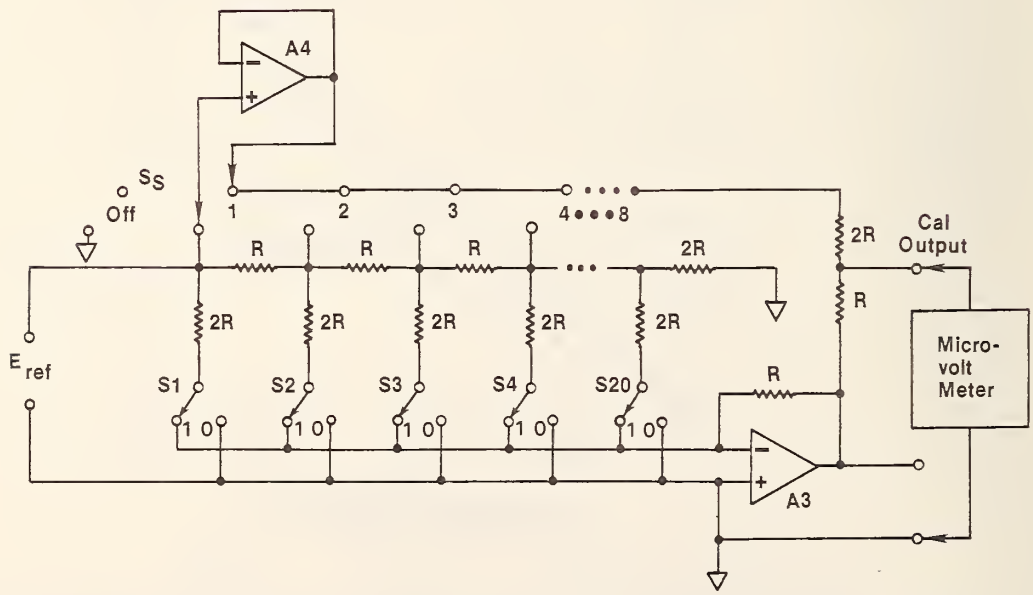

Fig. 6 Self-Calibration Circuit

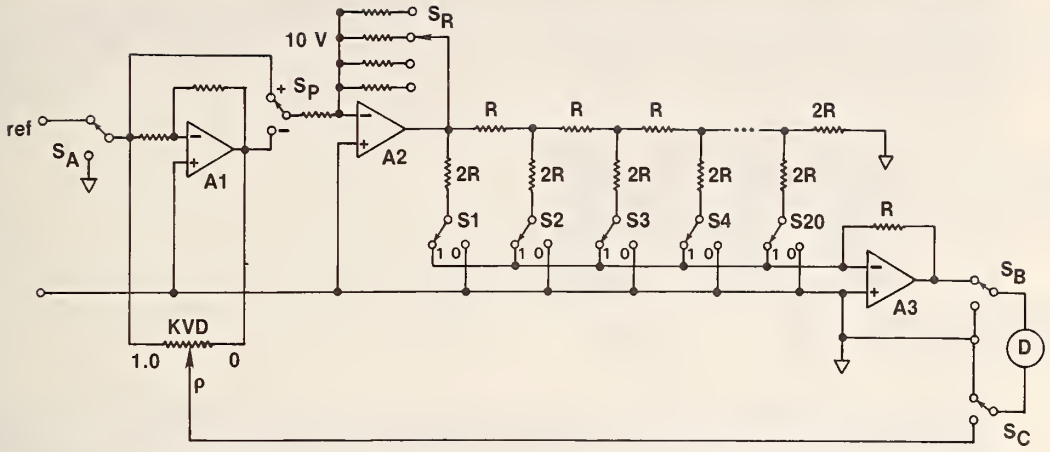

Fig. 7 Linearity Calibration Circuit

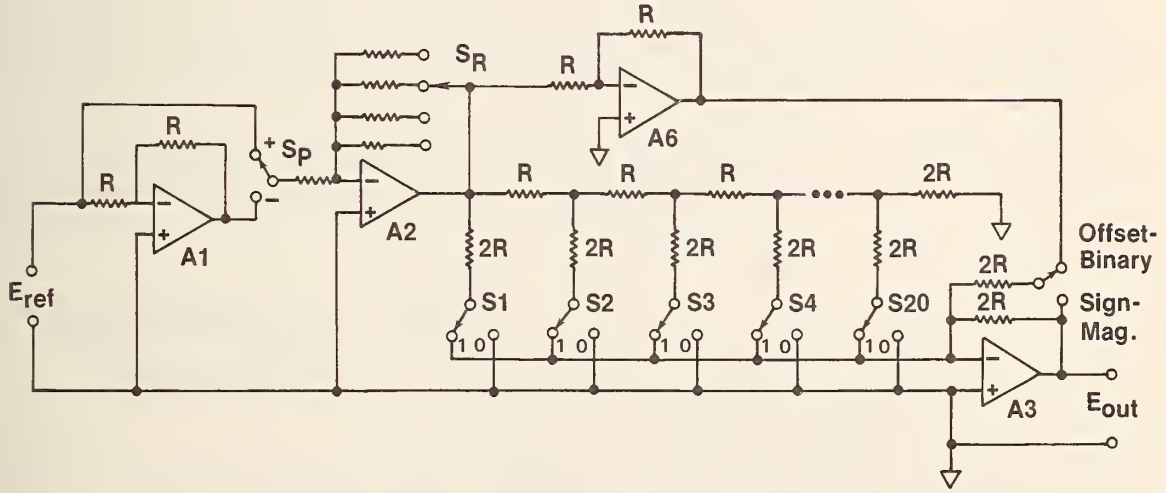

Fig. 8 Optional Offset Binary Coding

Fig. 9 Completed Instrument

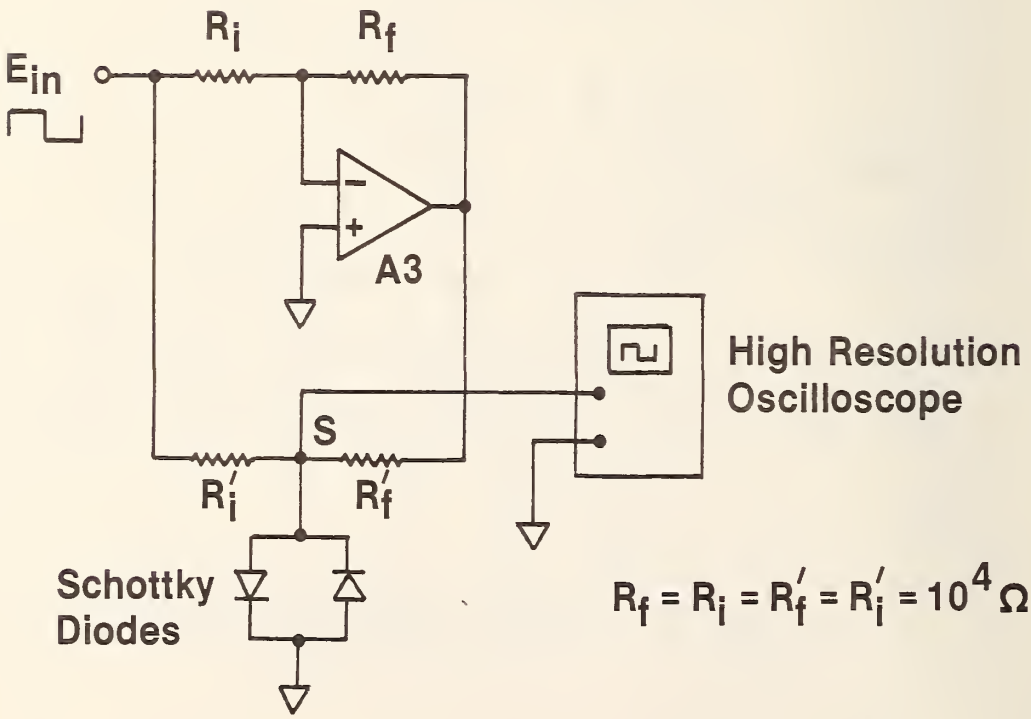

Fig. 10 Amplifier Settling Time Measurement

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14. Sponsoring Agency Code

15. SUPPLEMENTARY NOTES

☐ Document describes a computer program; SF-185, FIPS Software Summary, is attached.

16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

A multirange, 20-bit + sign, voltage output d/a converter is described. The converter exhibits less than 1 ppm (of full scale range) linearity error, and temperature coefficients of gain, offset and linearity of less than 0.5 ppm/°C. The design is based on the R-2R ladder network in the current steering mode, using miniature latching relays with mercury wetted contacts for switching. Ten buffered, temperature-controlled unsaturated standard cells comprise the voltage reference.

Techniques with design details are presented for minimizing errors due to relay thermal emf's, for implementing a self-calibration of linearity errors, and for obtaining optional coding formats. Calibration techniques are discussed and representative calibration data are presented.

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

Digital-to-analog converter; high resolution; multirange; R-2R ladder; relay switching; self-calibration; twenty bits + sign; voltage output

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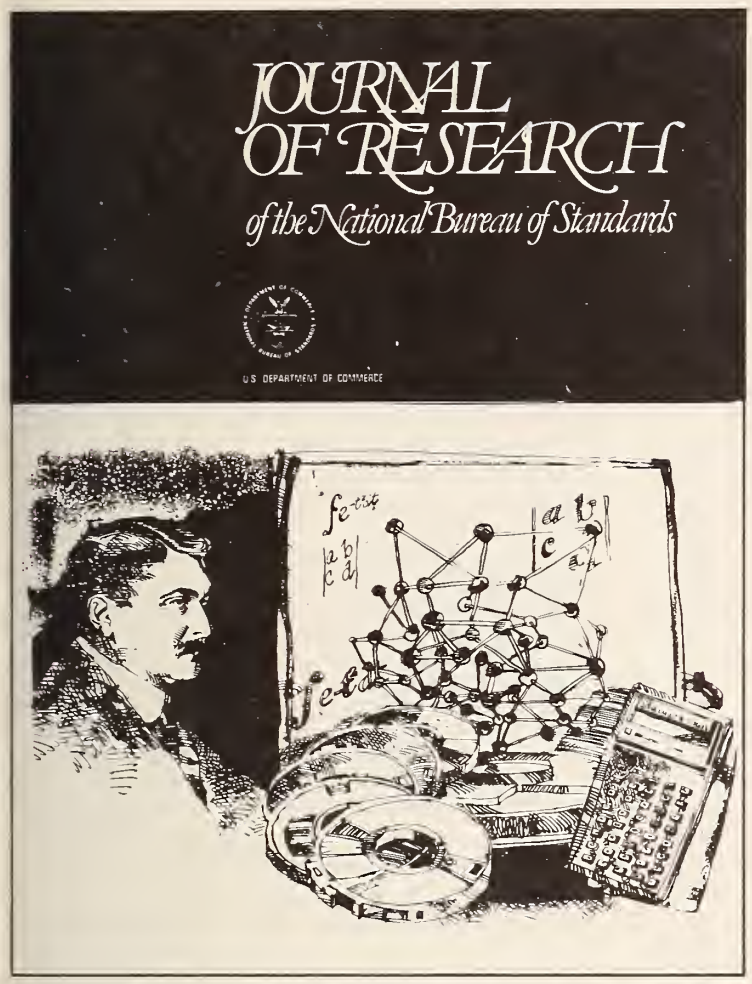

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